

Napatech Confirms Tier-1 SmartNIC Design Win Utilizing Latest Intel Technology

COPENHAGEN, Denmark – February 28, 2023 – Napatech[™] (OSLO: NAPA.OL), a leading provider of programmable Smart Network Interface Cards (SmartNICs) and Infrastructure Processing Units (IPU) used in cloud, enterprise and telecom datacenter networks today confirmed a new design win with <u>F5</u>, a global leader in multi-cloud application security and delivery solutions. The new design is powered by the latest technology from Intel, a global semiconductor leader and pioneer of FPGA-based SmartNICs and Infrastructure Processing Units.

With new cloud-native solutions based on the trusted <u>BIG-IP</u> platform, F5 simplifies telco infrastructure, creates new revenue opportunities with managed services, and reduces the complexity of multi-cloud and hybrid cloud deployments.

Napatech's complete solution delivers a production-grade SmartNIC based on the Intel FPGA SmartNIC N6000-PL Platform featuring an Intel Agilex 7 FPGA, meeting F5's rigorous requirements. Napatech's NT-400 family of programmable SmartNICs are available to original equipment manufacturers (OEM) for embedded designs, as well as end-users who are deploying software applications on standard servers. Napatech SmartNICs provide out-of-box benefits to applications and services which include cybersecurity, FinTech, and 5G mobile infrastructure including high performance for security functions, cloud services, and networking monitoring and recording.

At the core of the Napatech solution for F5 is Intel's newest technology, the Intel Agilex 7 FPGA with Ftile. Napatech chose the Intel Agilex 7 FPGA for a host of reasons, including scalability options that allowed support for five different options that meet various price, performance, power and feature configurations, tailored to specific customer applications and use cases. The Intel Agilex 7 FPGA also offers a broad set of capabilities that make it ideally suited for SmartNIC and IPU designs, including hardened Ethernet functions, PCIe 4.0 x 16, 400 Gbps of packet processing throughput, a wide range of interface options including 10/25/40/50/100/200 gigabit Ethernet, and 760 Gbps of memory bandwidth to support tensof-millions of simultaneous flows. Combined, these features enabled by the F-tile play a critical role in helping Napatech's SmartNIC design to operate within the space and power boundaries of high-volume standard server offerings.

"The global demand for computing that is fast, secure, efficient and sustainable is fueling the need for a rethink of traditional server architecture. This design win is a testament to the benefits of FPGA-based programmable NICs," said Vlad Galabov, Cloud and Data Center Research Director at Omdia. "Compute-intensive tasks like many security and network applications can be computed very efficiently on FPGAs. Napatech's software makes these processors easy to program and therefore more accessible to IT organizations."

"We are pleased to work with successful global companies like F5 whose solutions are reshaping the way networks are built, and Intel who is providing the underlying technology to bring it to life," said Jarrod Siket, chief marketing officer, Napatech. "This design win is another validation of our product strategy that aligns with the rapid growth in SmartNIC demand, and another step forward in unlocking value to our customers and shareholders."

"Operators rely on F5 as a critical infrastructure partner to deliver innovative 5G solutions with secure, resilient performance for hybrid and multi-cloud environments," said Geoff Petersen, Sr. Manager, Service



Provider Security Product Management, F5. "As experts in traffic management and security, we leverage performant FPGA hardware to help manage compute-intensive, high-volume offload—such as during a DDoS attack. We are excited to partner with Intel and Napatech while utilizing their leading technology to power our next generation product designs."

"This design-win with Napatech showcases the many benefits of Intel products for both OEM embedded designs, and end user deployments," said Mike Fitton, Vice President and General Manager, Network Business Division at Intel. "In particular, the design highlights the 2x fabric performance-per-watt advantage of Intel Agilex FPGAs, as compared to competing 7nm FPGAs available today¹."

¹ <u>https://edc.intel.com/content/www/us/en/products/performance/benchmarks/agilex-fpga/</u>

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About Napatech

Napatech is the leading supplier of SmartNIC solutions used in cloud, enterprise, and telecom datacenters. Through commercial-grade software suites integrated with high-performance hardware, Napatech accelerates network infrastructure and security workloads to deliver best-in-class system-level performance while maximizing the availability of server compute resources for applications and services. Additional information is available at: <u>www.napatech.com</u>.

No Forward-Looking Statements

This press release may contain forward-looking statements which are only predictions and may differ materially from actual future events or results due to a variety of factors, including but not limited to, business conditions, trends in the industry and markets, global economic and geopolitical conditions, macro-economic factors, and other risks and uncertainties set forth in Napatech's reports. The matter discussed in this release is based on current expectations and may be subject to change. Napatech will not necessarily update this information.

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